Engineering Electronics

A Practical Approach

Appendix A

Robert Mauro
Department of Electrical Engineering
Manhattan College

PRENTICE HALL
Englewood Cliffs
New Jersey 07632

numbers is the equivalent of the analog input voltage. The ramp-style A/D converter in effect determines this unknown number by asking the following series of questions in sequence: Is the number zero? Is the number one? Is the number two? and so on. It keeps on going until it gets a match at the comparator output. For example, if the final number found were $(157)_{10}$, then 157 clock cycles or guesses would be required to carry out this conversion. Clearly, this is not the most efficient way to proceed.

To find an unknown number between 0 and 255 with the smallest number of guesses, the best approach is first to guess a number halfway up, and determine whether the unknown number is above or below this point. Depending on the answer, we divide in half the upper or lower range that remains, and then ask whether the number is above or below this point. This series of questions is continued until the unknown number is found. As illustrated in the table in Figure 7.3-15a, asking the question "Is the unknown number greater than 128?", for example, is equivalent to the more subtle question "Is the MSB equal to 1?". The other questions have similar meanings.

This technique is known as successive approximation and it requires only n clock cycles to accomplish an n-bit A/D conversion. As a result, an 8-bit successive-approximation A/D converter, for example, is 32 times faster than an equivalent ramp-style A/D converter, while the hardware required for both is comparable (Figure 7.3-15b). The major difference between the two circuits is that the binary counter in the ramp-style A/D circuit has been replaced by a successive-approximation register (SAR).

This circuit operates as follows. On the first clock pulse the MSB (b_7) of the SAR is set equal to 1. If the comparator output stays high (as it does for the case under consideration in the figure), this bit is kept at a 1; if the comparator output goes low, the MSB is reset to zero by the SAR hardware. On the next clock pulse b_6 is set equal to 1, and as before, if the comparator output remains high, this bit is also kept at a logic 1. This procedure is repeated six more times by the SAR hardware, and after a total of eight clock cycles, this 8-bit A/D conversion is completed. The important circuit waveforms during the first few clock cycles are shown in Figure 7.3-15c, assuming that the analog input voltage is 1.57 V and that the D/A output voltage is 2.55 V when a count of $(255)_{10}$ is in the SAR.

Exercises

7.3-1 Find the CMRR of the subtractor circuit given in Figure 7.3-1b if $R_f = 100$ kΩ, $R_f' = 101$ kΩ, and $R_2 = R_2' = 1$ kΩ. (Hint: Do not use formulas. Instead, just calculate A_d and A_{cm} directly from the circuit.) *Answer* 80.2 dB

7.3-2 Derive an expression for the output from the D/A converter in Figure 7.3-13 if the resistor $2R$ at the input to the op amp is replaced by a short circuit. *Answer* $v_o = (R_f/R)V_{BB}$ [decimal equivalent of the n-bit binary code]/2^n

7.3-3 For the circuit shown in Figure 7.3-7a, $R = 500$ kΩ, $C = 1$ μF, and $v_{in} = 2 \sin 4\pi t$ V. Find v_o at $t = 2$ s. *Answer* 0.318 V

7.4 ACTIVE FILTERS

A filter may be defined as a circuit that is designed to pass a certain band of frequencies while attenuating all others. The range of frequencies allowed

through the filter is called its passband, and the range attenuated is known as its stopband. There are four major filter categories: low-pass, high-pass, band-pass, and band-elimination (or band-reject) filters. The magnitude response versus frequency for each of these filter styles is sketched in Figure 7.4-1. The phase response for each of these filters is assumed to be zero.

The filter frequency response curves illustrated in Figure 7.4-1 are all ideal, and no physically realizable filter can have precisely these characteristics, but by careful design it is possible to approach many of their attributes. Consider, for example, the design of a low-pass filter having characteristics similar to those illustrated in Figure 7.4-1a. Specifically, this filter has a flat gain response and zero phase shift in the passband, zero gain in the stopband, and an instantaneous transition from the passband to the stopband at the cutoff frequency, f_c. If this filter is constructed with lumped-circuit elements, its transfer function will be of the form

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$$H(s) = \frac{(a_0)A_o}{s^n + a_{n-1}s^{n-1} + \cdots + a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0} \qquad (7.4\text{-}1)$$

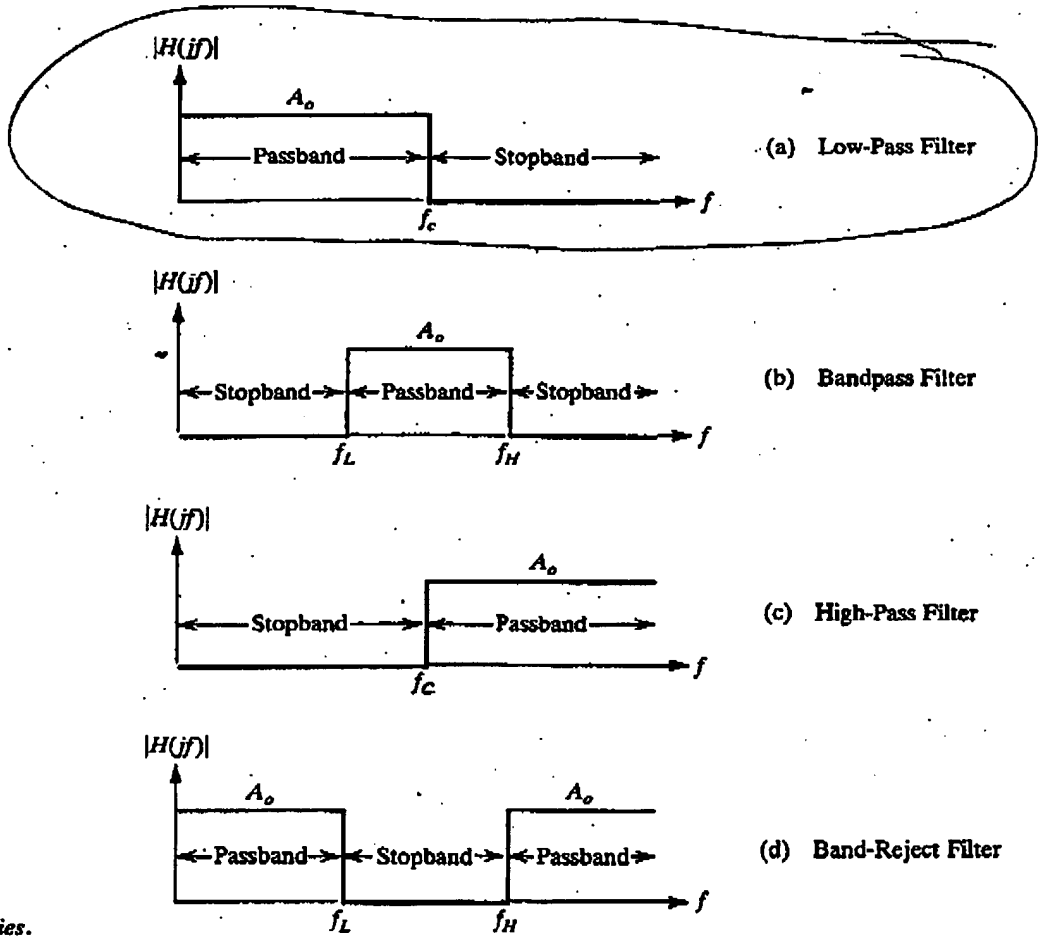

Figure 7.4-1
Basic filter categories.

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